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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/067,602	06/13/2011	Christopher William Laycock	JRL-550-1393	2606

73459 7590 11/30/2016

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ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
11/30/2016	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte CHRISTOPHER WILLIAM LAYCOCK,
ANTONY JOHN HARRIS, and ARTHUR LAUGHTON

Appeal 2015-007852
Application 13/067,602
Technology Center 2100

Before DEBRA K. STEPHENS, IRVIN E. BRANCH, and
DAVID J. CUTITTA II, Administrative Patent Judges.

CUTITTA, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 1–29.[1] We have jurisdiction over this appeal under 35 U.S.C. § 6(b).

We REVERSE.

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[1] Claims 1, 16, 26, 27, 28, and 29 are independent.

STATEMENT OF THE CASE

According to Appellants[2], the application relates to maintaining coherence of data when a cache memory is used to supplement main memory and when a legacy transaction master is not configured to perform snooping to ensure data coherency. Spec. 12.[3] Claim 1 is illustrative and is reproduced below with disputed limitations emphasized:

1. Memory interface apparatus comprising:

first interface circuitry configured to connect to transaction master circuitry;

second interface circuitry configured to connect to a memory system; and

transaction control circuitry coupled to said first interface circuitry and said second interface circuitry and configured to:

receive from said transaction master circuitry via said first interface circuitry a first write request to write target data associated with a memory address within said memory system;

issue via said second interface circuitry a further transaction request associated with said memory address;

receive via said second interface circuitry an indication of completion of said further transaction request;

issue via said second interface circuitry a second write request to write at least said write target data to said memory system;

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[2] According to Appellants, the real party in interest is ARM Limited.

[3] Throughout this Opinion, we refer to: (1) Appellants' Specification filed June 13, 2011 (Spec.); (2) the Final Office Action (Final Act.) mailed Aug. 14, 2014; (3) the Appeal Brief (Appeal Br.) filed Jan. 20, 2015; (4) the Examiner's Answer (Ans.) mailed June 29, 2015; and (5) the Reply Brief (Reply Br.) filed Aug. 28, 2015.

receive via said second interface circuitry a write response signal indicating said write target data has been written to said memory system; and

in dependence upon receipt of said write response signal, issue an acknowledge signal via said second interface circuitry to said memory system indicating said indication of completion associated with said further transaction and said write response signal have been received.

REFERENCES

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Laycock et al. ("Laycock")	US 2009/0319707 Al	Dec. 24, 2009

Dan Tang, Yungang Bao, Weiwu Hu, and Mingyu Chen, *DMA Cache: Using On-Chip Storage to Architecturally Separate I/O Data from CPU Data for Improving I/O Performance*, Key Laboratory of Computer System and Architecture, Institute of Computing Technology, Chinese Academy of Sciences (2009) (hereinafter "Tang").

REJECTION

Claims 1–29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang and Laycock. Final Act. 3.

Our review in this appeal is limited only to the above rejection and issues raised by Appellants. We have not considered other possible issues that have not been raised by Appellants and which are, therefore, not before us. *See* 37 C.F.R. § 41.37(c)(1)(iv) (2014).

ISSUE

Did the Examiner err in finding that the combination of Tang and Laycock teaches or suggests "in dependence upon receipt of said write response signal, issue an acknowledge signal via said second interface circuitry to said memory system indicating said indication of completion associated with said further transaction and said write response signal have been received," as recited in claim 1?

ANALYSIS

The Examiner relies upon the combination of Tang and Laycock to teach or suggest the disputed limitations of claim 1. Final Act. 4–5 and 9; Ans. 3. More specifically, the Examiner states:

> Laycock teaches "issu[ing] an acknowledge signal . . . indicating said indication of completion associated . . . said write response signal have been received" in [Para 94 LINES 12–13; "[this] write acknowledgement signal is passed for all write transactions"]. The optimal word there is "all" meaning whenever there is a write in either direction an acknowledgement would be sent. "Said further transaction" is taught by Tang in the form of a snoop [Fig 2], and therefore post the snoop taught by Tang, Laylock [*sic*] teaches an acknowledgement verifying a write has occurred. Laycock is not relied upon to tech [*sic*] the further transaction as the reference is relied upon to teach the acknowledgement signal. The teaching of the snoop as a further transaction by Tang and the teaching of the acknowledgement signal post a write taught by Laycock, in combination, teach the limitation in question.

Ans. 3.

Appellants contend the Examiner's findings are in error because Laycock does not have the correct *dependence* upon previously received signals to serve as the "acknowledge signal" of claim 1. Appeal Br. 22.

Specifically, Appellants contend "[t]he claims thus define the timing at which the claimed acknowledge signal is issued – 'in dependence upon receipt of said write response signal.'" Reply Br. 2. Appellants further contend the combination fails to teach or suggest "in dependence upon receipt of said write response signal," as claimed, because "neither Laycock nor Tang requires the acknowledgement signal to be held back until a write response signal in response to the 'Memory Write' in Figure 2 of Tang has also been received" and because "the Examiner maps the single one 'write acknowledge signal' of Laycock to both the claimed 'write response signal' and the claimed 'acknowledge signal' of claim 1." Appeal Br. 21; Reply Br. 3.

We agree with Appellants the Examiner has not demonstrated these findings are supported by the teachings or suggestions of Tang and Laycock. The Examiner indicates that Tang's snoop suggests the claimed "further transaction" and Laycock teaches, following the snoop, "issuing an acknowledge signal" associated with the snoop because Laycock teaches passing an acknowledgement signal for all write transactions. Ans. 3 ("post the snoop taught by Tang, Laylock [*sic*] teaches an acknowledgement verifying a write has occurred."). As Appellants argue, and we agree, the Examiner has not pointed to a disclosure in Tang or Laycock that teaches or suggests suppressing issuance of the acknowledgement signal *until* the claimed write response signal has been received. App. Br. 9; Reply Br. 6. Although we agree with the Examiner that Laycock teaches passing a write acknowledgement signal for all write transactions (Laycock ¶ 94), the Examiner fails to explain how this suggests "issu[ing] an acknowledge signal . . . indicating said indication of completion associated with said

further transaction" (Tang's snoop) "in dependence upon receipt of said write response signal," as recited in claim 1. That is, the Examiner's rationale does not specifically link the issuance of the indication of completion associated with Tang's further transaction with Laycock's teaching of a write response signal.

Accordingly, because we are unable to ascertain the basis in Tang or Laycock for the disputed findings discussed above, we are constrained to reverse the Examiner's 35 U.S.C. § 103(a) rejection of claim 1.[4]

Because we agree with at least one of the dispositive arguments advanced by Appellants for claim 1, we need not reach the merits of Appellants' other contentions. We express no opinion as to whether independent claim 1 would be obvious over Tang and Laycock if supported by additional explanation and/or references. We leave any such further consideration to the Examiner.

We also are constrained to reverse the rejection of independent claims 16, 26, 27, 28, and 29, which recite commensurate limitations, and of dependent claims 2–15 and 17–25, which stand with their respective independent claims.

DECISION

We reverse the Examiner's decision rejecting claims 1–29 under 35 U.S.C. § 103(a).

REVERSED

[4] In the event of further prosecution, the Examiner should ascertain whether there is sufficient antecedent basis for the limitation "said further transaction" in independent claims 1, 16, 26, 27, 28, and 29.